WITH MARKINGS TO SHOW CHANGES MADE".

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example by independent claim 1, and similarly claims 22 and 58-61, is directed to an electrically conductive layer having a copper alloy, which includes at least one of Bi, Sb, and Ti at not less than 0.1 percent by weight. The copper alloy has a melting point less than copper. (See Page 13, lines 5-13)

Separately, as disclosed and claimed, for example by independent claim 12, the copper alloy can also include at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight. (See Page 16, lines 5-10).

Devices depict interconnection structures formed in semiconductor devices of various materials, including aluminum, and with different structural dimensions and arrangements. However, a device generally has a trench groove with a narrow width, which "suppresses the growth of the copper crystal grain, whereby the copper crystal grain is likely to have a small size." The small size of the crystal grain allows existence of many crystal grain boundaries" reducing the reliability of the interconnection and the yield of the semiconductor device. (See Page 5, lines 19-22; and Page 6, lines 1-5).

An important aspect of the copper alloy is that it includes at least one of Bi, Sb, and Ti at not less than 0.1 percent by weight. Further, the copper alloy could also include at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight. These features suppress the mass-transfer of copper through the copper alloy and prevent the resistivity of the copper alloy from becoming too high. (See Page 13, lines 5-13; Page 16, lines 5-23; Page 23, lines 5-15; and Page 40, lines 4-21).

As a result of this invention, the resultant structure, including the electrically conductive layer, the copper alloy has relatively large crystal grain sizes and reduced crystal grain boundaries in a current flow direction. Thus, a reduction in electromigration of an interconnection layer in a semiconductor device is produced decreasing the probability of disconnection and cracking of the interconnection layer, thereby improving the reliability and productivity of the semiconductor device.(See Page 6, line 10 - Page 7, line 16; Page 13, lines 17-24; and Page 54, lines 1-10).

II. THE PRIOR ART REJECTION

The § 103(a) Rejection of Claims 1-37 and 57-63

First, the references, separately, or in combination, fail to teach, disclose or provide a reason or motivation for being combined. In particular, Tsuji, et al. ("Tsuji") pertains to a method of manufacturing a film carrier having leads comprising a resin base film and a rolled copper foil laminated on the film used for mounting semiconductor chips or other electrical components in place and achieving greater packaging densities. (See Tsuji at Abstract; Column 1, lines 5-11).

Tsuji is specifically directed to improving the strength and heat resistance of the leads

by reducing their thickness and eliminating the anisotropy, i.e., unequalness, of their mechanical properties "with the ability of being etched with increased accuracy and meeting the growing requirement for high-density multipin arrangements." (See Column 3, lines 26-37). Accordingly, Tsuji teaches that the rolled copper foil is made of copper alloy compositions where the copper foil is photo-etched to provide copper inner leads and outer leads with testing pads. Both the inner leads and the outer leads form an interface between external circuits and electrode terminals of a semiconductor chip. (See Column 1, lines 20-25 and lines 48-68; Column 2, lines 8-17; Column 3, lines 52-58; and Figure 1).

By contrast, Edelstein, et al. ("Edelstein") does not have the same aim as Tsuji. Instead, Edelstein discloses a copper interconnection structure incorporating a metal seed layer for providing electrical connections with an electronic device where either a copper alloy seed layer or a metal seed layer of Ag, Mo, W, or Co is sandwiched between a copper conductor body and an electronic device. (See Edelstein at Abstract; Column 1, lines 5-13; and Column 6, lines 10-23).

Edelstein, therefore, is concerned with "improving the electromigration resistance, the adhesion and the surface properties of the interconnection structure" not strength and heat resistance of leads as with Tsuji. (See Column 1, lines 10-15; and Column 6, lines 10-23). Nothing within Edelstein suggests a rolled copper foil made of a copper alloy composition where the copper foil is photo-etched to provide copper inner leads and outer leads with testing pads. Thus, Tsuji teaches away from being combined with another invention, such as, Edelstein.

By contrast, Dubin also does not have the same aim as either Tsuji or Edelstein. Instead, Dubin discloses a copper or copper alloy interconnection pattern formed by a

damascene technique where aluminum or magnesium alloy is deposited in a damascene opening formed in a dielectric layer. Copper or a copper alloy is electroplated or electrolessly plated on the aluminum or magnesium alloy. (See Dubin at Abstract; Column 1, lines 5-10). Accordingly, the "aluminum or magnesium atoms diffuse through the copper or copper alloy and accumulate on its surface forming a self-encapsulated oxide." (See Dubin at Abstract).

Dubin, therefore, is concerned in the semiconductor technology area with "enabling the formation of Cu or Cu alloy metallization in interconnection patterns with improved corrosion resistance while substantially reducing or eliminating Cu diffusion" in order to improve manufacturing of high speed integrated circuits having submicron design features and high conductivity interconnect structures. (See Dubin at Abstract; Column 1, lines 5-10; Column 3, lines 57-62). Nothing within Dubin suggests a rolled copper foil made of a copper alloy composition where the copper foil is photo-etched to provide copper inner leads and outer leads with testing pads. Thus, Tsuji also teaches away from being combined with another invention, such as, Dubin.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight. It is clear that the Examiner has simply read Applicant's specification and conducted a keyword search to yield Tsuji, Edelstein and Dubin. Accordingly, Applicant traverses the Examiner's characterization of the cited references in accordance with the above analysis. Further, the Examiner provides no motivation or reason to combine other than to assert that it would be obvious to one having ordinary skill in the art at the time to combine the references of interconnection structure as being "well-known." Tsuji, however, has nothing to do with interconnection structures within layers of a semiconductor. Accordingly, such an assertion does not take into account the distinct method and related structural differences of

the inventions as indicated above, and further discussed below. Thus this assertion attempts to solve a potential problem which does not exist with Tsuji.

Second, Tsuji does not teach or suggest the features of independent claim 1, and similar claims 58-61, including an electrically conductive layer composed of a copper alloy, which includes at least one of Bi, Sb, and Ti at not less than 0.1 percent by weight, wherein said copper alloy has a melting point less than copper. (See Page 13, lines 5-13).

Rather, Tsuji discloses a conventional method for manufacturing a film carrier including rolled copper foil made of a copper alloy composition where the copper foil is photo-etched to provide copper inner leads and outer leads with testing pads. Both the inner leads and the outer leads form an interface between external circuits and electrode terminals of a semiconductor chip. (See Column 1, lines 20-25 and lines 48-68; Column 2, lines 8-17; Column 3, lines 52-58; and Figure 1). The copper alloy consists of one or more elements, including Ag, As, P and Si at 0.05-0.2 wt % but not Bi, Sb and Ti. Since Tsuji teaches that the wt. % is at least less than 0.1 wt. %, Tsuji's copper alloy will have relatively small crystal grain sizes and many crystal boundaries, which is consistent with Tsuji's goal of reduced lead thickness. (See Application, Page 24, lines 18-24; and Tsuji, Column 3, lines 26-37).

Consequently, Tsuji's conventional method is unsuitable for achieving at least two objects of the invention, which include effectively producing a copper alloy with relatively large crystal grain sizes and reduced crystal grain boundaries in a current flow direction which suppress the mass-transfer of copper through the copper alloy and prevents the resistivity of the copper alloy from becoming too high. (See Page 6, line 10 - Page 7, line 16; Page 13, lines 5-13 and 17-24; Page 16, lines 5-23; Page 23, lines 5-15; Page 40, lines 4-21; and Page 54, lines 1-10). Tsuji does not teach, suggest or disclose an electrically conductive layer composed of a copper alloy, which includes at least one of Bi, Sb, and Ti at not less than 0.1

percent by weight, wherein said copper alloy has a melting point less than copper. (See Page 13, lines 5-13). Edelstein does not remedy the deficiencies of the Tsuji.

Secondly, Edelstein similarly to Tsuji discussed above fails to teach or suggest an electrically conductive layer composed of a copper alloy, which includes at least one of Bi, Sb, and Ti at not less than 0.1 percent by weight, wherein said copper alloy has a melting point less than copper as recited in claim 1. Edelstein also fails to teach or suggest a copper alloy which includes at least one of Mo, Ta, and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight as recited in claim 12.

Rather Edelstein discloses, in part, a copper interconnection structure incorporating a metal seed layer for providing electrical connections with an electronic device where either a copper alloy seed layer or the metal seed layer of Ag, Mo, W, or Co is sandwiched between a copper conductor body and an electronic device. (See Edelstein at Abstract; Column 1, lines 5-13; and Column 6, lines 10-23). Edelstein teaches that copper alloy seed layers may be formed from a variety of elements, including Ag, Si, Ti and P. (See Column 8, lines 30-33). However, Edelstein does not provide any percentage of weight of the alloy elements, let alone a percentage of weight of less than 0.1 percent by weight. Edelstein, accordingly, does not teach a copper alloy, which includes at least one of Bi and Sb at not less than 0.1 percent by weight, wherein said copper alloy has a melting point less than copper as recited in claim 1, and similar claims 22 and 59-61. (See Column 6, lines 30-50; and Column 8, lines 30-45).

In addition, Edelstein also teaches that the copper seed layer, or the metal seed layer of Ag, Mo, W or Co, has a thickness in the range of 0.1 nm-100 nm but does not disclose any percent by weight for any of these elements in the alloy, or any of the other disclosed elements, including Ti, let alone the critical percentage weight range of Applicant's invention. (See Column 9, lines 38-45). As indicated, Applicant's invention discloses that the copper alloy

includes at least one of Mo, Ta, and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight. Applicant, accordingly, indicates that this range is critical to the invention as previously discussed above regarding Tsuji and separate independent claim 1. In particular, the presence of any of these elements in the copper alloy greater than 1 percent causes the resistivity of the copper alloy to be too high and the resistance of the interconnection to be too high. (See Page 40, lines 4-7).

Similarly, the presence of these elements in the copper alloy less than 0.1 percent by weight has the effect of insufficiently suppressing the mass-transfer of copper through the copper, which results in disconnection and cracking of the interconnection and insufficient reliability of the semiconductor device containing the interconnection. (See Page 40, lines 8-21). Thus, Applicant disagrees with the assertion in the Office Action that Edelstein's copper alloy seed layer or metal seed layer can be used to produce Applicant's invention.

Consequently, Edelstein's conventional structure is also unsuitable for achieving at least two objects of the invention, which include effectively producing a copper alloy with relatively large crystal grain sizes and reduced crystal grain boundaries in a current flow direction which suppress the mass-transfer of copper through the copper alloy and prevents the resistivity of the copper alloy from becoming too high. (See Page 6, line 10 - Page 7, line 16; Page 13, lines 5-13 and 17-24; Page 16, lines 5-23; Page 23, lines 5-15; Page 40, lines 4-21; and Page 54, lines 1-10). Edelstein, therefore, also does not teach, suggest or disclose a copper alloy which includes at least one of Mo, Ta, and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight as recited in claim 12.

Dubin also does not remedy the deficiencies of either Tsuji or Edelstein.

Thirdly, Dubin similarly to Tsuji and Edelstein discussed above fails to teach or suggest an electrically conductive layer composed of a copper alloy, which includes at least

one of Bi, Sb, and Ti at not less than 0.1 percent by weight, wherein said copper alloy has a melting point less than copper as recited in claim 1, and similar claim 58. Dubin also fails to teach or suggest a copper alloy which includes at least one of Mo, Ta, and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight as recited in claim 12, and similar claim 60.

Rather Dubin discloses, in part, a copper or copper alloy interconnection pattern formed by a damascene technique where aluminum or magnesium alloy is deposited in a damascene opening formed in a dielectric layer. Copper or a copper alloy is electroplated or electrolessly plated on the aluminum or magnesium alloy. (See Dubin at Abstract; Column 1, lines 5-10). Since Dubin teaches that the copper alloy seed layer may be formed from a variety of elements, including Ag, Mg, Sn, Zn, Pd, Au, Zr and Ni, Dubin does not teach a copper alloy, which includes at least one of Bi, Sb and Ti at not less than 0.1 percent by weight, wherein said copper alloy has a melting point less than copper as recited in claim 1. (See Column 5, line 66; Column 6, lines 48-50 and Column 8, lines 30-45).

In addition, Dubin also teaches a diffusion barrier layer composed of a variety of elements and alloys, in particular, Ta, Ta alloys, Wa, Was alloys, Si, Ti and Ti alloys. (See Column 7, lines 13-18). However, these elements and alloys comprise a diffusion barrier layer to protect against diffusion of Cu atoms from the Cu metallization though dielectric layer not an electrically conductive layer as disclosed in Applicant's invention, let alone an electrically conductive layer including a copper alloy as indicated in claim 12 of Applicant's invention. Dubin also does not disclose any percent by weight of any of these elements, let alone the percentage range of Applicant's invention. (See Column 9, lines 38-45). As indicated, Applicant's invention discloses that the copper alloy includes at least one of Mo, Ta, and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight. Applicant,

accordingly, indicates that this range is important to the invention as discussed above. Absent these elements falling within this range either the resistivity of the copper alloy and interconnection becomes too high or the mass-transfer of copper through the copper is insufficiently suppressed, which results in disconnection and cracking of the interconnection yielding insufficient reliability of the semiconductor device containing the interconnection. (See Page 40, lines 4-21).

Thus, Applicant disagrees with the assertion in the Office Action that Dubin's copper alloy seed layer or diffusion layer can be used to produce Applicant's invention. Consequently, Dubin's conventional structure is also unsuitable for achieving at least two objects of the invention, which include effectively producing a copper alloy with relatively large crystal grain sizes and reduced crystal grain boundaries in a current flow direction which suppress the mass-transfer of copper through the copper alloy and prevents the resistivity of the copper alloy from becoming too high. (See Page 6, line 10 - Page 7, line 16; Page 13, lines 5-13 and 17-24; Page 16, lines 5-23; Page 23, lines 5-15; Page 40, lines 4-21; and Page 54, lines 1-10). Dubin, therefore, also does not teach, suggest or disclose a copper alloy which includes at least one of Mo, Ta, and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight as recited in claim 12.

For at least the reasons outlined above, Applicant respectfully submits that Tsuji, Edelstein or Dubin, separately or in combination, do not teach or suggest all of the features of independent claims 1, 12, 22, 30 and 57-61, and related dependent claim 2-11, 13-21, 23-29, 31-37 and 62-63.

Finally, regarding the dependent claims 2-11, 13-21, 23-29 and 31-37 and 62-63, which depend from claims 1, 12, 22, 30 and 61, these claims are patentable not only by virtue of their dependency from their independent claims but also by the additional limitations they

recite.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-37 and 57-63 all the claims presently pending in the application are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 9/12/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

1. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of [Ag, As,] Bi, [P,] Sb, [Si] and Ti at not less than 0.1 percent by weight,

wherein said copper alloy has a melting point less than copper.

22. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an insulation layer over said semiconductor substrate, and said insulation layer having a trench groove;

a barrier metal layer on a bottom and side walls of said trench groove; and

an electrically conductive layer provided in an interconnection layer on said barrier metal layer, and said interconnection layer filling said trench groove,

wherein said interconnection layer comprises a copper alloy which includes at least one of [Ag, As,] Bi, [P,] Sb, [Si] and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution.

57. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of [As,] Bi, [P,] Sb, [Si] and Ti at more than 0.2 percent by weight,

said copper alloy formed on a substrate of said semiconductor circuit.

58. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of Bi, [P,] Sb and Ti at not less than 0.1 percent by weight,

said copper alloy formed on a substrate of said semiconductor circuit.

59. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of [Ag, As,] Bi,[P,] Sb, [Si] and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution,

said copper alloy formed on a substrate of said semiconductor circuit.

60. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of [Ag, As,] Bi, [P,] Sb, [Si] and Ti at not less than 0.1 percent by weight and at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight,

wherein said copper alloy has a melting point less than copper and the mass-transfer of copper is suppressed through said copper alloy.

61. (Amended) An electrically conductive layer provided in a semiconductor circuit comprising:

a copper alloy which includes at least one of [Ag, As,] Bi,[P,] Sb, [Si] and Ti at not less than 0.1 percent by weight,

said copper alloy provided in a groove within an inter-layer formed on a substrate of said semiconductor circuit.